IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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For: COMBINED PHASE COMPARATOR AND CHARGE PUMP CIRCUIT

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RESPONSE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Response is being filed in response to the Office Action mailed from the U.S. Patent and Trademark Office on July 13, 2004 in the above-identified application. Reconsideration and further examination are requested.

Applicant notes with appreciation the finding that claims 2-4, 7-9, 12, 14, 16 and 18 would be allowed if rewritten in independent form. However, those claims have not been rewritten because it is believed that the base claims are allowable for the reasons presented below.

Claims 1, 5-6, 10-11, 13, 15 and 17 were rejected under 35 U.S.C. 102(e) as being anticipated by O'Sullivan et al. (U.S. patent 6,259,755). That rejection is respectfully traversed and reconsideration is requested.

As discussed in prior responses, and with reference to Figure 14, the present invention relates to a multiplier circuit that generates an output signal bclk at a rate that is a multiple of an input signal aclk. To that end, a phase comparator 191 directly compares the phase of an edge of an input signal with the phase of an edge of the output signal, that is, through the top feedback loop of Figure 14. Prior art circuits such as illustrated in Figure 16 have not directly compared the two signals but, rather, have inserted a divider 193 between the output and the phase comparator. The divider generated a signal from the output for comparison with the input signal, the generated signal being of the same frequency as the input signal.

The O'Sullivan et al. reference does not relate to a multiplier circuit and does not suggest generating "an output signal at a rate that is a multiple of input frequency of an input signal." As can be seen in Fig. 13 of O'Sullivan et al., the recovered output clock 1202, which is generated by the VCO 1109 and fed back to the phase comparator 1104, has the same frequency as the data of the input data signal 1200A. Compare the clock pulses of signal 1202 with the zeros and ones at the top of the figure.

In the claimed multiplier circuit, the generated output signal has a higher rate than the input signal and thus a number of transitions which can not be compared to the input signal. In the embodiment recited in, for example, claims 2 and 7, only limited ones of the transitions of the output signal are selected by a window signal to be compared to the lower frequency input signal. By contrast, in O'Sullivan et al., both signals have the same underlying frequency, and comparisons are made at the data transitions that are identified by window signal 1204A. The window signal of the claimed invention can be generated directly from the output through a divider (for example, claims 3 and 8); whereas, O'Sullivan et al. requires a data transition detector that monitors the data input.

In conclusion, O'Sullivan et al. does not teach the claimed "multiplier" having "an output signal at a rate that is a multiple of input frequencies of an input signal" and, thus, does not anticipate the claimed invention. Nor would one would look to a data recovery circuit, which compares transitions of a data signal with a recovered clock at the same frequency as the data, to derive a multiplier circuit that generates an output signal at a rate that is a multiple of the input frequency of an input signal.

In view of the above remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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